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ORIGINAL RESEARCH

Asymmetric modulation of bridgeless single-stage full-bridge AC–DC converter for active power factor correction and zero voltage switching

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Abstract

Singe-phase single-stage AC–DC converters exhibit the advantages of lower cost, higher efficiency, and lower power semiconductor device count compared with traditional two-stage topologies. However, most existing single-stage AC–DC topologies encounter some or all the following drawbacks: hard-switching operation, bulky bus or output capacitor, uncontrolled bus voltage, not actively shaped input current, a large amount of power semiconductor devices, etc. The bridgeless single-stage full-bridge AC–DC converter can be considered a promising solution for high power capacity and efficiency. However, this topology still suffers from most of the drawbacks. In this paper, a new asymmetric modulation method of bridgeless single-stage full-bridge AC–DC converter is proposed to achieve active power factor (PF) correction and zero-voltage switching. Topology description, the proposed modulation and control methods, theoretical analysis progress, and reference design procedure are presented in detail. Finally, a 2-kW laboratory prototype is implemented with experimental results presented to validate the principle and design.

1 | INTRODUCTION

Single-stage AC–DC converters attract much attention because of lower cost, higher efficiency, lower power semiconductor device count, and lower control complexity. Single-stage flyback and forward-based converters [1–10] usually utilize the lowest count of power semiconductor devices. However, due to hard switching and higher voltage stress, they are restrictedly used in low-power (< 100 W) applications, such as LED drivers. Single-stage half-bridge converters [11–20] utilize a low count of power semiconductor devices and reduce the production cost, also suitable for low-power applications.

Currently, there are emerging demands of high-power AC–DC converters for various industrial applications such as electric vehicle (EV) charger and power supply unit for large-scale data centre. Single-stage resonant converters [13, 16, 18, 20, 21] and full-bridge converters [21– 32] are the most used single-stage topologies for high-power applications because of the soft-switching characteristics. However, the single-stage resonant converters suffer from the problem of large frequency variation range, resulting in complexity and difficulty in magnetic components design. Some researchers proposed single-stage three-level converters [33, 34] to reduce the power semiconductor devices' voltage stress; however, the topologies are more

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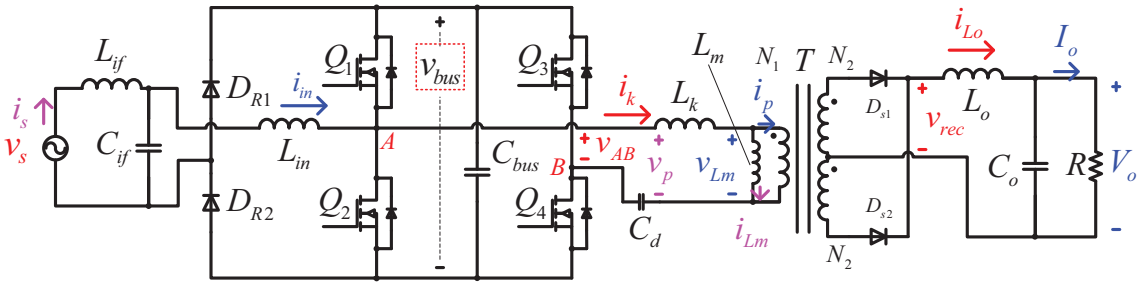

FIGURE 1 Bridgeless single-stage full-bridge AC–DC converter

complicated with a high count of power semiconductor devices and auxiliary windings, which increase the cost and power losses. Single-stage current-fed full-bridge converters [35, 36] were proposed to increase the input power factor (PF), eliminate the DC bus capacitor, and achieve soft-switching. However, the lack of energy-storage DC bus capacitors may result in high-voltage overshoots and ringing across the DC bus side. Also, if without large output electrolytic capacitors, there will be a large double-line frequency ripple. Moreover, such single-stage current fed converters require a relatively large number of power semiconductor devices which increases the conduction loss and production cost. Among the abovementioned single-stage topologies, some converters [6, 11, 12, 17– 24, 29] apply bridgeless rectifier instead of full-bridge diode rectifier at the front end to increase the system efficiency furtherly (by reducing the conduction loss) and decrease the count of power diodes. In general, the bridgeless single-stage full-bridge AC–DC converters can be considered a promising solution for high-power AC–DC conversion aiming for higher efficiency and lower cost.

However, the existing modulation methods [21, 22, 24, 25, 29, 30] of the bridgeless single-stage full-bridge AC–DC converters still suffer from several significant drawbacks. The three-level symmetric modulation methods proposed in [22, 24, 25, 29] would come across the zero current cross distortion problem of AC input current, which is an intrinsic limitation problem. Researchers of [21] also apply the three-level symmetric modulation method. However, it has two significant drawbacks: an uncontrolled and fluctuant bus voltage, and a large output capacitor. This is because it only has one control variable for the whole system, which is used to shape and control the AC input current only. Hence, it does not have another control variable to control the output voltage. It inevitably generates a large double-line frequency ripple to the secondary side, and it must use a large and bulky output capacitor to absorb the ripple. The modulation method in [30] is applied for the bridgeless single-stage full-bridge AC–DC wireless power transfer converter, which applies a fixed duty cycle to control the AC input current over the AC line cycle at a specific load condition. Although it does not have the problem of zero current cross distortion, the total harmonic distortion (THD) of the AC input current is still not sufficiently low because the AC input current is naturally shaped, and it inherently contains a degree of higher-order harmonics. Moreover, it only uses one control variable for both AC input current and output voltage; hence, a large bus or output capacitor is required, and the bus voltage may be excessive for light load or standby conditions.

In this paper, a novel asymmetric modulation method for the bridgeless single-stage full-bridge AC–DC converter is proposed with the advantages of (1) actively shaped AC input current with a low THD and a high PF; (2) soft-switching operations for all switches; (3) reduced DC bus and output capacitances; and (4) stable and controlled bus voltage.

In this paper, the proposed modulation method and topology description are presented in Section 2 and the design procedure and implementation of the laboratory prototype are given in detail in Section 3. Finally, the experimental results verify the principle, analysis, and design in Section 4.

2 | PROPOSED TOPOLOGY, MODULATION, AND CONTROL

2.1 | Topology description

Figure 1 shows the bridgeless single-stage full-bridge AC–DC converter, which utilizes a full-bridge structure to achieve both AC–DC power factor correction (PFC) and DC–DC isolated conversion simultaneously. v_s is the AC input voltage (with input current noted as i_s), L_{if} and C_{if} are the inductor and capacitor of the input filter, D_{R1} and D_{R2} are the front-end bridgeless rectifier diodes, L_{in} is the input inductor, C_{bus} is the bus capacitor, Q_1 to Q_4 are four MOSFET switches (with body diodes D_1–D_4), C_d is the DC-blocking capacitor, L_k is the primary-side inductor, T is the transformer (with magnetic inductance L_m and ratio n (N_2/N_1)), D_{s1} and D_{s2} are secondary-side rectifier diodes, L_o and C_o are the output inductor and capacitor, and R is the load resistor. Usually, a bulky electrolytic capacitor is used as the bus capacitor or output capacitor to reduce the bus voltage's ripple in traditional two-stage AC–DC converters or other single-stage topologies. For the proposed topology, the double-line frequency ripple is allowed to exist in the bus voltage v_{bus} (voltage across C_{bus}); therefore, the polypropylene capacitors with much smaller capacitance and volume are used as C_{bus} and C_o, respectively.

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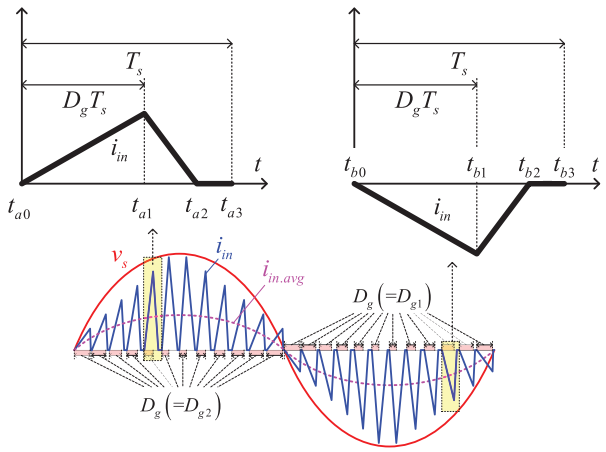

FIGURE 2 Schematic waveform of i_{in} of the AC–DC bridgeless PFC rectifier part

2.2 | AC–DC bridgeless PFC rectifier part with the proposed asymmetric modulation method

For the proposed topology, v_{g1} to v_{g4} refer to the gate-source (GS) voltage of switches Q_1 to Q_4, respectively; v_{Q1} to v_{Q4} refer to the drain-source (DS) voltage of switches Q_1 to Q_4, respectively. D_{g1} to D_{g4} are defined as the duty cycles of v_{g1} to v_{g4}, respectively. v_{AB} is defined as the full-bridge voltage. D_g is defined equal to D_{g2} when v_s is positive (equal to D_{g1} when v_s is in its negative cycle). There are two diodes D_{R1} and D_{R2}, two switches Q_1 and Q_2, an input inductor L_{in}, and a bus capacitor C_{bus} forming the bridgeless boost PFC rectifier; when operating in discontinuous current mode (DCM) with a constant D_g, it can perform PFC functions. However, the THD is not satisfactory because the input current is naturally shaped.

In this paper, an active PFC control method is proposed to reduce bus voltage, improve power quality furtherly, and eliminate bulky bus capacitor. The average input inductor current $i_{in.avg}$, working in DCM, is controlled to follow v_s to improve the power quality. Therefore, D_g is varying with v_s with a double-line frequency at steady state.

Figure 2 shows the schematic waveform of the input inductor current i_{in} when v_s is in its both positive and negative cycles.

For positive v_s condition, when switch Q_2 is turned on, the voltage across L_{in} is v_s, and the input current i_{in} flowing through L_{in} is positively increasing from zero. When switch Q_2 is turned off, the voltage across L_{in} is v_s to v_{bus}, and the input current i_{in} flowing through L_{in} is positively decreasing to zero. For positive v_s condition, i_{in} within a switching period T_s can be expressed as

$$i_{in}|_{v_s\geq 0}=\begin{cases}\dfrac{v_s}{L_{in}}\cdot t & t_{a0}\leq t<t_{a1}\\ \dfrac{v_s}{L_{in}}\cdot t_{a1}+\dfrac{v_s-v_{bus}}{L_{in}}\cdot(t-t_{a1}) & t_{a1}\leq t<t_{a2}\\ 0 & t_{a2}\leq t<t_{a3}\end{cases}\quad(1)$$

where t_{a0}, t_{a1}, t_{a2}, and t_{a3} are defined as

$$t_{a0}=0, t_{a1}=D_{g2}T_s, t_{a2}=D_{g2}T_s\cdot\frac{v_{bus}}{v_{bus}-v_s}, t_{a3}=T_s\quad(2)$$

where D_{g2} is the turn-on duty cycle of switch Q_2.

For negative v_s condition, when switch Q_1 is turned on, the voltage across L_{in} is v_s, and the input current i_{in} flowing through L_{in} is negatively increasing from zero. When switch Q_1 is turned off, the voltage across L_{in} is $v_s + v_{bus}$, and the input current i_{in} flowing through L_{in} is negatively decreasing to zero. For negative v_s condition, i_{in} within a switching period T_s can be expressed as

$$i_{in}|_{v_s<0}=\begin{cases}\dfrac{v_s}{L_{in}}\cdot t & t_{b0}\leq t<t_{b1}\\ \dfrac{v_s}{L_{in}}\cdot t_{b1}+\dfrac{v_s+v_{bus}}{L_{in}}\cdot(t-t_{b1}) & t_{b1}\leq t<t_{b2}\\ 0 & t_{b2}\leq t<t_{b3}\end{cases}\quad(3)$$

where t_{b0}, t_{b1}, t_{b2}, and t_{b3} are defined as

$$t_{b0}=0, t_{b1}=D_{g1}T_s, t_{b2}=D_{g1}T_s\cdot\frac{v_{bus}}{v_s+v_{bus}}, t_{b3}=T_s\quad(4)$$

where D_{g1} is the turn-on duty cycle of switch Q_1.

Hence, for positive v_s condition, D_{g2} controls i_{in}, while for negative v_s condition, D_{g1} controls i_{in}. To unify the two conditions, D_g is defined as the duty cycle when there is only v_s applied across the AC input inductor L_{in}, and i_{in}'s absolute value is increasing from zero. Hence, for positive v_s half cycle, D_g is equal to D_{g2}. For negative v_s half cycle, D_g is equal to D_{g1}. For the requirement of i_{in} DCM operation, t_{a2} should be smaller than or equal to t_{a3}, and t_{b2} should be smaller than or equal to t_{b3}. Hence, from (1) to (4), D_g is limited as

$$\begin{cases}D_gT_s\cdot\dfrac{v_{bus}}{v_{bus}-v_s}\leq T_s, & v_s\geq 0\\ D_gT_s\cdot\dfrac{v_{bus}}{v_s+v_{bus}}\leq T_s & v_s<0\end{cases}\Rightarrow D_g\leq\frac{v_{bus}-|v_s|}{v_{bus}}\quad(5)$$

The average value of i_{in} over a switching period T_s is defined as $i_{in.avg}$ and can be calculated from (1) to (4), expressed as

$$i_{in.avg}=\frac{v_sv_{bus}D_g^2}{2L_{in}f_s(v_{bus}-|v_s|)}\quad(6)$$

where f_s is defined as the switching frequency.

To actively shape the AC input current to be sinusoidal, $i_{in.avg}$ is required to follow the variation of v_s:

$$i_{in.avg}=k_{iv}\cdot v_s\quad(7)$$

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where k_{iv} is the ratio of $i_{in.avg}$ and v_s. Therefore, the relation between D_g and v_s is obtained as

$$D_g = \sqrt{2L_{in}f_s k_{iv} \cdot \frac{v_{bus} - |v_s|}{v_{bus}}} \tag{8}$$

From (5) and (8), the meaningful range of k_{iv} is obtained as

$$0 \le k_{iv} \le \frac{1}{2L_{in}f_s} \cdot \left(\frac{v_{bus} - |v_s|}{v_{bus}}\right)_{\min} \tag{9}$$

For a given k_{iv}, the maximum and minimum values of D_g are

$$D_{g\min} = \sqrt{k_{iv} \cdot 2L_{in}f_s} \cdot \left(\sqrt{\frac{v_{bus} - |v_s|}{v_{bus}}}\right)_{\min}$$
$$D_{g\max} = \sqrt{k_{iv} \cdot 2L_{in}f_s} \tag{10}$$

From (8), D_g is the function of v_s, v_{bus}, and k_{iv}. At steady state, k_{iv} is constant while v_s and v_{bus} fluctuate with line and double-line frequencies respectively. The bridge leg of Q_1 and Q_2 is controlled by D_g to shape the AC input current, while the bridge leg of Q_3 and Q_4 is controlled to shape the waveform of v_{AB}. Therefore, the waveform of v_{AB} is controlled varying over the line period to maintain constant output voltage and remove the double-line-frequency ripple in the output voltage.

2.3 | Full-bridge DC–DC isolated converter part with the proposed asymmetric modulation method

The DC–DC isolated converter part consists of a full-bridge inverter, a DC-blocking capacitor C_d, a primary-side inductor L_k, a transformer T, secondary-side diodes D_{s1} and D_{s2}, and output inductor and capacitor (L_o and C_o).

Figure 3 presents the key ideal operation waveforms. v_{AB} is modulated as an asymmetric three-level waveform and D_a refers to the negative-level duty cycle while D_b refers to the positive-level one. D_a and D_b are two independent control variables to regulate output voltage V_o.

As defined in Figure 1, v_p is also considered the AC component of v_{AB}. v_{Lm} refers to the voltage across the magnetic inductance L_m of T. v_{rec} is defined as the voltage across the DC-port of the secondary-side diode-rectifier and V_o is defined as the output voltage. V_m is defined as the middle level of v_p, calculated as

$$V_m = v_{bus}(D_a - D_b) \tag{11}$$

i_k, i_{Lm}, and i_p are defined as the currents related to the primary side of T, as shown in Figure 1. i_{Lo} is defined as the current flowing through L_o. I_o is defined as the output current. From Figure 3, V_a, V_b, and V_c are defined as the corresponding voltages of v_{Lm} during t_1 to t_2, t_4 to t_5, t_5 to t_6, and t_2 to t_3,

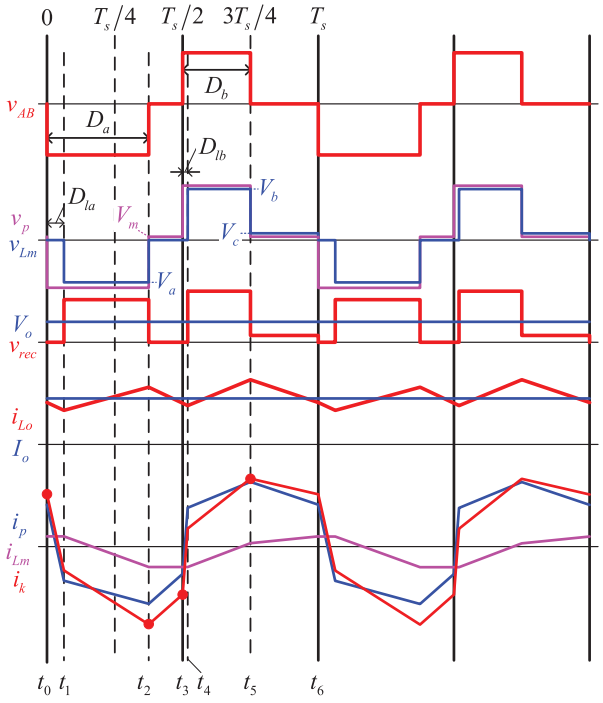

FIGURE 3 Operation waveforms of full-bridge DC–DC isolated converter with the proposed asymmetric modulation method

respectively. D_{la} and D_{lb} are defined as the lost duties of D_a and D_b, respectively.

The following analysis is based on the condition of $D_a \ge D_b$. The characteristics of the condition of $D_a < D_b$ are symmetric with those of $D_a > D_b$. Hence, the analysis processes of the condition of $D_a < D_b$ are omitted.

There are two preliminary assumptions required to be stated before the following analysis. Firstly, the reflected output inductor L_o/n^2 is much larger than the primary-side inductor L_k

$$\frac{L_o}{n^2} \gg L_k \tag{12}$$

Secondly, the output inductor current i_{Lo} is required to work in continuous current mode (CCM). Then, L_o is limited as

$$L_o \ge \left\{ \begin{array}{l} \frac{1}{2}\left[\frac{1+(D_a-D_b)}{V_o/(nV_{bus})}\frac{L_m}{L_k+L_m} - 1\right] D_b T_s R, \\ \frac{1}{2}\left[1 - \frac{D_a-D_b}{V_o/(nV_{bus})}\frac{L_m}{L_k+L_m}\right](0.5-D_b)\, T_s R \end{array} \right\}_{\max} \tag{13}$$

By analysis, V_a, V_b, V_c, D_{la}, and D_{lb} are calculated as

$$V_a = -v_{bus}(1-(D_a-D_b))(L_m/(L_k+L_m)) \tag{14}$$

$$V_b = v_{bus}(1+(D_a-D_b))(L_m/(L_k+L_m)) \tag{15}$$

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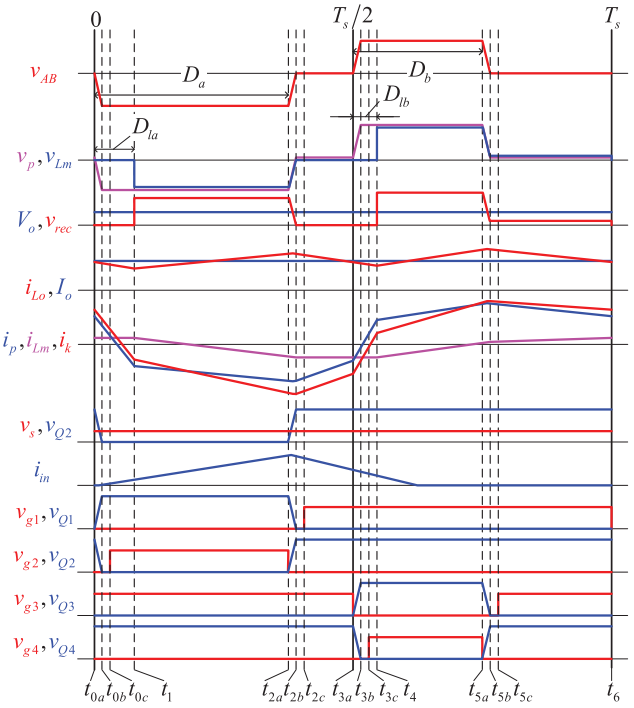

FIGURE 4 Operation waveforms within a switching period

$$V_c = v_{bus}\,(D_a - D_b)\,(L_m/(L_k + L_m)) \tag{16}$$

$$D_{la} = \frac{2nL_k f_s I_o}{v_{bus}\,(1 - (D_a - D_b))} \tag{17}$$

$$D_{lb} = \frac{2nL_k f_s I_o}{v_{bus}\,(1 + (D_a - D_b))} - \frac{(D_a - D_b)\,(0.5 - D_a)}{(1 + (D_a - D_b))} \tag{18}$$

Finally, the normalized voltage transfer gain from v_{bus} to V_o is analyzed and calculated as

$$\frac{V_o}{nv_{bus}} = \frac{(D_a + D_b) - (D_a - D_b)^2 + (D_a - D_b)\,(1 - (D_a + D_b))}{1 + L_k/L_m + 4n^2 L_k/(RT_s)} \tag{19}$$

2.4 | Operation modes

Figure 4 shows the operation waveforms in a specific condition, and it is taken as an example to explain the operation modes within a switching period. The operation mode of each time interval is presented in Figure 5.

Stage 1 (t_{0a}–t_{0c}): At t_{0a}, Q_1 is turned off. C_{s1} starts to be charged by i_k while C_{s2} starts to be discharged by i_k. At t_{0b}, C_{s1} is charged to v_{bus} while C_{s2} is discharged to zero. At this instant, D_2 starts to conduct. During t_{0a} to t_{0b}, v_s starts to be larger than v_{Q2} and i_{in} starts to flow. At t_{0c}, v_{Q2} has been zero, and Q_2 is turned on. Q_1' is turning off and Q_2' is turning on to realize zero-voltage-switching (ZVS).

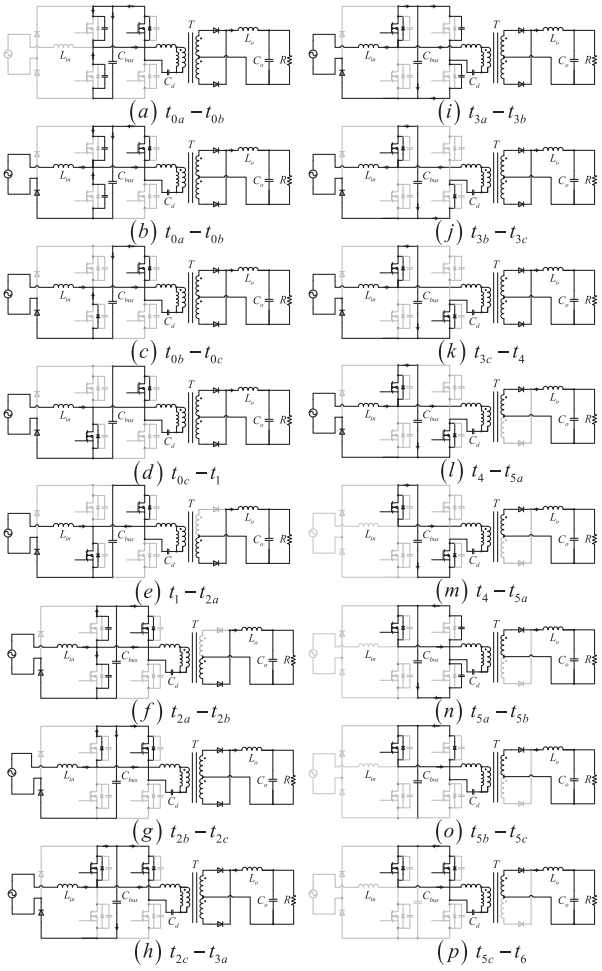

FIGURE 5 Operation modes in a switching period. (a) t_{0a} to t_{0b}, (b) $t_{0a}$to t_{0b}, (c) t_{0b} to t_{0c}, (d) t_{0c} to t_1, (e) t_1 to t_{2a}, (f) t_{2a} to t_{2b}, (g) t_{2b} to t_{2c}, (h) t_{2c} to t_{3a}, (i) t_{3a} to t_{3b}, (j) t_{3b} to t_{3c}, (k) t_{3c} to t_4, (l) t_4 to t_{5a}, (m) t_4 to t_{5a}, (n) t_{5a} to t_{5b}, (o) t_{5b} to t_{5c}, (p) t_{5c} to t_6

Stage 2 (t_{0c}–t_{2a}): From t_{0c} to t_{2a}, Q_2 and Q_3 are on whereas Q_1 and Q_4 are off. Since t_{0a}, i_p has been transiting from positive to negative until t_1.

Stage 3 (t_{2a}–t_{2c}): At t_{2a}, Q_2 is turned off. C_{s2} starts to be charged by i_{in} and i_k while C_{s1} starts to be discharged by i_{in} and i_k. During t_{2a} to t_{2b}, v_s starts to be smaller than v_{Q2} and i_{in} starts to decrease. At t_{2b}, C_{s2} is charged to v_{bus} while C_{s1} is discharged to zero. At this instant, D_1 starts to conduct. At t_{2c}, v_{Q1} has been zero, and Q_1 is turned on. Q_2 is turning off and Q_1 is turning on to realize ZVS.

Stage 4 (t_{2c}–t_{3a}): During t_{2c} to t_{3a}, Q_1 and Q_3 are on, whereas Q_2 and Q_4 are off.

Stage 5 (t_{3a}–t_{3c}): At t_{3a}, Q_3 is turned off. C_{s3} starts to be charged by i_k and i_{in} while C_{s4} starts to be discharged by i_k and i_{in}. At t_{3b}, C_{s3} is charged to v_{bus} while C_{s4} is discharged to zero. And D_4 starts to conduct. At t_{3c}, v_{Q4} has been zero, and Q_4 is turned on. Q_3 is turning off and Q_4 is turning on to realize ZVS.

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Stage 6 (t_{3c}–t_{5a}): From t_{3c} to t_{5a}, Q_1 and Q_4 are on whereas Q_2 and Q_3 are off. Since t_{3a}, i_p has been transiting from negative to positive until t_4. At a time within t_4 to t_{5a}, i_{in} decreases to zero.

Stage 7 (t_{5a}–t_{5c}): At t_{5a}, Q_4 is turned off. C_{s4} starts to be charged by i_k while C_{s3} starts to be discharged by i_k. At t_{5b}, C_{s4} is charged to v_{bus} while C_{s3} is discharged to zero. At this instant, D_3 starts to conduct. At t_{5c}, v_{Q3} has been zero, and Q_3 is turned on. Q_4 is turning off and Q_3 is turning on to realize ZVS.

Stage 8 (t_{5c} – t_6): From t_{5c} to t_6, Q_1 and Q_3 are on whereas Q_2 and Q_4 are off.

2.5 | Soft-switching (zero-voltage-switching) analysis

The following analysis is also based on the condition of $D_a \geq D_b$. By analyzing the behaviours of i_p, i_{Lm}, and i_k, a series of equations and inequations can be obtained:

$$I_{p.dc} = -I_{Lm.dc} \tag{20}$$

$$I_{p.dc} \geq nI_o\left(D_{la} - D_{lb}\right) \tag{21}$$

$$I_{Lm3} = \begin{bmatrix} I_{Lm.dc} + \dfrac{V_a\left(D_a - D_{la}\right)\left(0.5 + D_{la} + D_a - D_b\right)}{2L_m f_s} \\ -\dfrac{V_b\left(D_b - D_{lb}\right)\left(0.5 - D_{lb}\right)}{2L_m f_s} \end{bmatrix} \tag{22}$$

$$I_{k3} = I_{p3} + I_{Lm3} \tag{23}$$

$$I_{p3} = -nI_{Lo2} + \frac{V_m}{L_k}\left(0.5 - D_a\right)T_s \tag{24}$$

$$I_{Lo2} \geq I_o \tag{25}$$

where $I_{p.dc}$ and $I_{Lm.dc}$ are defined as the DC components of i_p and i_{Lm}, respectively. I_{k3}, I_{p3}, and I_{Lm3} are defined as the instantaneous values of i_k, i_p, and i_{Lm} at t_3, respectively. I_{Lo2} is defined as the instantaneous value of i_{Lo} at t_2. From (20) to (25), an inequation of I_{k3} is obtained

$$\begin{aligned} I_{k3} \leq\ & -nI_o\left(1 + D_{la} - D_{lb}\right) + \frac{V_m}{L_k f_s}\left(0.5 - D_a\right) \\ & + \frac{V_a}{2L_m f_s}\left(D_a - D_{la}\right)\left(0.5 + D_{la} + D_a - D_b\right) \\ & - \frac{V_b}{2L_m f_s}\left(D_b - D_{lb}\right)\left(0.5 - D_{lb}\right) \end{aligned} \tag{26}$$

From Figure 3, I_{k3} is the key current of ZVS operation, and it must be negative. Finally, the ZVS requirements are expressed as

$$I_{crit} = \begin{bmatrix} nI_o\left(1 + D_{la} - D_{lb}\right) - \dfrac{V_m\left(0.5 - D_a\right)}{L_k f_s} \\ -\dfrac{V_a\left(D_a - D_{la}\right)\left(0.5 + D_{la} + D_a - D_b\right)}{2L_m f_s} \\ +\dfrac{V_b\left(D_b - D_{lb}\right)\left(0.5 - D_{lb}\right)}{2L_m f_s} \end{bmatrix}_{\min} > 0 \tag{27}$$

$$\frac{2C_s v_{bus}}{0.5I_{crit}} \leq T_{dt} \tag{28}$$

where I_{crit} is defined as the critical current of ZVS. T_{dt} is the switching deadtime between the upper and lower switches of a bridge leg. Q_1 to Q_4's snubber capacitors are designed with the same capacitance C_s.

2.6 | PWM generation of Q_1 to Q_4

When D_{g2} is smaller than or equal to 0.5, D_{g4} is also controlled to be smaller than or equal to 0.5, vice versa. The switching characteristics of Q_1 and Q_3 are complementary with those of Q_2 and Q_4, and hence the switching waveforms of Q_1 and Q_3 are omitted. For AC–DC bridgeless rectifier part, the control variable D_g is directly related to D_{g2}:

$$\begin{cases} D_g = D_{g2}, & v_s \geq 0 \\ D_g = 1 - D_{g2}, & v_s < 0 \end{cases} \tag{29}$$

For the DC–DC converter part, it can also be observed that D_a and D_b have the relationship with D_{g2} and D_{g4}:

$$\begin{cases} D_a = D_{g2}, D_b = D_{g4}, & D_{g2}, D_{g4} \leq 0.5 \\ D_a = 1 - D_{g4}, D_b = 1 - D_{g2}, & D_{g2}, D_{g4} > 0.5 \end{cases} \tag{30}$$

2.7 | Bus voltage analysis

v_s is assumed to be sinusoidal and defined as

$$v_s = V_{sp}\sin\left(\omega_l t\right) \tag{31}$$

where V_{sp} is the peak value of v_s. By analyzing the power balancing relationship between the input, bus capacitor, and output, the bus capacitor energy equation is obtained as

$$\frac{1}{2}C_{bus}{v_{bus}}^2 = -\frac{k_{iv}{V_{sp}}^2}{4\omega_l}\sin\left(2\omega_l t\right) + \frac{1}{2}C_{bus}{V_{bus.\text{avg}}}^2 \tag{32}$$

Therefore, v_{bus} is expressed as

$$v_{bus} = \sqrt{{V_{bus.\text{avg}}}^2 - \frac{k_{iv}{V_{sp}}^2}{2\omega_l C_{bus}}\sin\left(2\omega_l t\right)} \tag{33}$$

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where η is defined as the efficiency of the converter. $V_{bus.avg}$ is defined as the average value of v_{bus} within a switching period.

2.8 | Control strategy of the single-stage topology

V_o is controlled to be constant at steady state by adjusting D_a or D_b while AC–DC PFC functionality is achieved by adjusting D_g. In other words, D_g and v_{bus} are periodically varying because of the AC–DC PFC part. From (8), D_g is controlled and varying with the changing v_s and v_{bus} to control i_{in} following v_s and achieve PFC. D_b is defined as another intermediate parameter (related to duty cycles of v_{g3} and v_{g4}) to shape the waveform of v_{AB}. D_b is controlled and varying with the periodically changing D_g and v_{bus} to maintain V_o constant. As aforementioned, D_a refers to the negative duty cycle of v_{AB} while D_b refers to the positive one. The relations between $\{D_{g1}$–$D_{g4}\}$ and $\{D_g, D_b\}$ are summarized as

$$\begin{cases} D_{g1} = 1 - D_g, D_{g2} = D_g, D_{g3} = 1 - D_b, D_{g4} = D_b, & v_s \geq 0 \\ D_{g1} = D_g, D_{g2} = 1 - D_g, D_{g3} = D_b, D_{g4} = 1 - D_b, & v_s < 0 \end{cases} \tag{34}$$

Combining (30) and (34), the relations between $\{D_a, D_b\}$ and $\{D_g, D_b\}$ are derived as

$$\begin{cases} D_a = D_g, D_b = D_b, & v_s \geq 0 \text{ and } D_g, D_b \leq 0.5 \\ D_a = D_b, D_b = D_g, & v_s < 0 \text{ and } D_g, D_b \leq 0.5 \\ D_a = 1 - D_b, D_b = 1 - D_g, & v_s \geq 0 \text{ and } D_g, D_b > 0.5 \\ D_a = 1 - D_g, D_b = 1 - D_b, & v_s < 0 \text{ and } D_g, D_b > 0.5 \end{cases} \tag{35}$$

The normalized voltage transfer gain from $V_{bus.avg}$ to V_o is

$$G_{v.s} = \frac{V_o}{nV_{bus.avg}} = \frac{V_o}{nv_{bus}} \cdot \frac{v_{bus}}{V_{bus.avg}} = \frac{k_{out}}{1 + L_k/L_m + 4n^2 L_k/(RT_s)} \tag{36}$$

where k_{out} is defined as the control variable to maintain constant V_o in different load conditions. When D_g and D_b are smaller than or equal to 0.5, k_{out} is expressed as

$$k_{out} = \left[\begin{matrix} (D_g + D_b) - (D_g - D_b)^2 \\ + \left| D_g - D_b \right| (1 - D_g - D_b) \end{matrix} \right] \frac{v_{bus}}{V_{bus.\text{avg}}} \tag{37}$$

when D_g and D_b are larger than 0.5, k_{out} is expressed as

$$k_{out} = \left[\begin{matrix} (2 - D_g - D_b) - (D_g - D_b)^2 \\ + \left| D_g - D_b \right| (D_g + D_b - 1) \end{matrix} \right] \frac{v_{bus}}{V_{bus.\text{avg}}} \tag{38}$$

Figure 6 shows the schematic diagram of the proposed control strategy, which can be realized by DSP F28335 controller integrated with AD modules and PWM generation modules. $v_{bus.meas}$, $v_{s.meas}$, and $V_{o.meas}$ are defined as measured values of v_{bus}, v_s, and V_o. Then $V_{bus.avg}$ and V_{sp} could be calculated by averaging $v_{bus.meas}$ and the absolute values of $v_{s.meas}$ with half a line period. The time t is synchronized by detecting the cross-zero point (negative to positive) of $v_{s.meas}$.

The control target is to maintain the average bus voltage $V_{bus.avg}$ and the output voltage V_o constant in different load conditions. Hence, a double closed-loop control method is applied to maintain $V_{bus.avg}$ and V_o simultaneously, as shown in Figure 6b. k_{iv} and k_{out} designed to regulate the input current and output voltage respectively. The first control loop (noted as output voltage loop) applies a proportional-integral (PI) compensation module with a faster dynamic response to control V_o equal to $V_{o.ref}$ while the second control loop (noted as the bus voltage loop) applies a PI compensation module with a slower dynamic response to control $V_{bus.}$avg equal to $V_{bus.}$avg.ref., $V_{bus.}$avg.ref, and $V_{o.ref}$ are defined as the reference values of $V_{bus.}$avg and V_o.

Figure 6c shows the flowchart of generation of D_{g1} to D_{g4}, with the compensated k_{iv} and k_{out}. According to the processed sampled signals $V_{bus.avg}$, V_{sp}, and t, the instantaneous values of v_s and v_{bus} are estimated using (31) and (33), respectively. Then, to achieve PFC, the instantaneous D_g of a specific switching period is calculated from (8) with the estimated v_s and v_{bus}, and the compensated k_{iv}. For the calculation of D_g, the estimated v_s and v_{bus} help to shape the envelope of the input current while k_{iv} controls the magnitude of the input current. The constant V_o within a line period is achieved by actively estimating the instantaneous v_{bus} using the processed sample signals $V_{bus.avg}$, V_{sp}, and t. According to v_{bus}, $V_{bus.avg}$, D_g, and k_{out}, the appropriate D_b to output constant V_o could be calculated using (37) or (38). For the calculation of D_b, the estimated v_{bus}, processed sampled $V_{bus.avg}$, and previously calculated D_g help to eliminate the double-line ripple of the output voltage while k_{out} controls the output voltage level. Finally, the duty cycles of the switches Q_1 to Q_4 can be obtained with D_g and D_b using (34).

2.9 | Other considerations

A bus voltage coefficient k_{bus} is defined as the ratio of v_{bus} and $V_{bus.avg}$. k_{bus} is also regarded as a function of time t if (33) holds. From (8), D_g is the function of v_s, also regarded as the function of time t. G_v is the function of D_g and D_b, and therefore regarded as the function of time t and D_b. At the steady state, $V_o/V_{bus.}$avg is constant and hence k_{out} needs to be controlled constant. The following condition is required:

$$\left[\frac{k_{out}}{1 + L_k/L_m + 4n^2 L_k f_s/R} \bigg|_{D_b = 0.5} \right]_{\min} \geq \frac{V_o}{nV_{bus.avg}} \tag{39}$$

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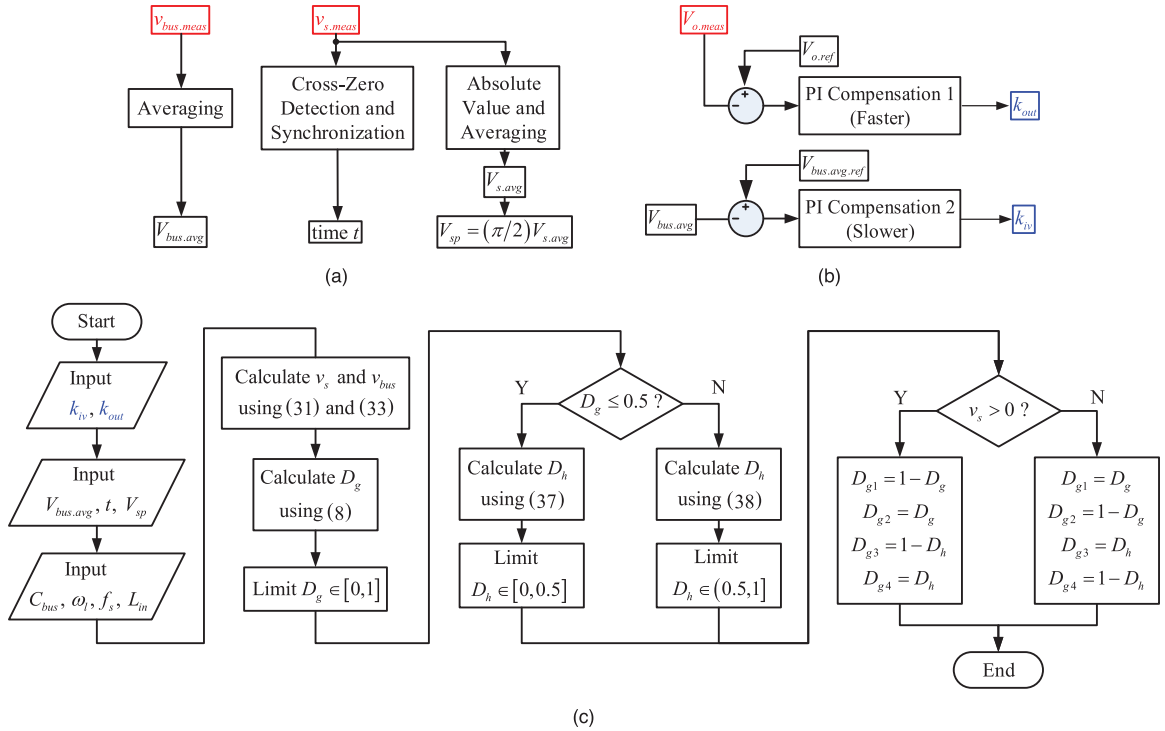

FIGURE 6 Schematic diagram of the proposed control strategy: (a) signal processing part to generate $V_{bus.avg}$ and V_{sp}, and synchronized time t; (b) double closed-loop control part to generate control variables k_{iv} and k_{out}; (c) flowchart of switches' driving duty cycles generation with compensated k_{iv} and k_{out}

From (5) and (8), the range of k_{iv} is revised as

$$0 \le k_{iv} \le \frac{1}{2L_{in}f_s} \cdot \left(1 - \frac{V_{sp}}{V_{bus.\mathrm{avg}}} \cdot \frac{|\sin(\omega_l t)|}{k_{bus}(t)}\right)_{\min} \tag{40}$$

3 | DESIGN PROCEDURE AND LABORATORY PROTOTYPE

A laboratory prototype is implemented. The corresponding hardware setup and detailed design procedure are presented.

3.1 | Input, output, and bus voltage requirements

Input voltage v_s is confirmed to be 50 Hz 220 V_{rms} AC power source from power grid, and the allowable fluctuant voltage range is from 198 to 242 V_{rms} (10% fluctuation range). Output voltage V_o is designed to be 200 V and maximum (rated) output power $P_{o.\max}$ is 2 kW. Therefore, maximum output current $I_{o.max}$ is 10 A and the corresponding load resistance is 20 Ω. The average bus voltage $V_{bus.\mathrm{avg}}$ is designed to be 600 V.

Note the efficiency of the converter as η and hence

$$\frac{P_o}{\eta} = P_{in} = \frac{k_{iv}V_{sp}^2}{2} \tag{41}$$

In maximum load condition, assuming η is 92%, when v_s is 198 V_{rms}, the corresponding k_{iv} (noted as $k_{iv.1}$) is calculated to be 0.055. When v_s is 242 V_{rms}, the corresponding k_{iv} (noted as $k_{iv.2}$) is calculated to be 0.037. $k_{iv.1}$ is also considered the maximum k_{iv} value for different input and load conditions.

3.2 | Selection of bus capacitor C_{bus}, operation frequency f_s, and input inductor L_{in}

From (40) and (41), in maximum load condition, the product of L_{in} and f_s is limited as

$$L_{in}f_s \le \frac{\eta V_{sp.\min}^2}{4P_{o.\max}} \left(1 - \frac{V_{sp.\min}}{V_{bus.\mathrm{avg}}} \sqrt{1 + \frac{1}{\left(\frac{\eta\omega_l C_{bus} V_{bus.\mathrm{avg}}^2}{P_{o.\max}}\right)^2 - 1}}\right) \tag{42}$$

C_{bus} is designed as 240 μF. According to (42), f_s is selected to be 50 kHz and L_{in} is designed to be 95.0 μH.

3.3 | Selection of L_{k}, L_{m}, and n

L_k, L_m, and n are designed according to the minimum allowable load condition, which is denoted as K_{L_min}. For this prototype, K_{L_min} is set as 20%. The following analysis and calculation are based on K_{L_min}. In K_{L_min} load condition, η is assumed as 87%.

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Firstly, for different line input conditions, from (10), (31), (33), and (41), the minimum and maximum values of D_g are calculated 0.179 and 0.334, respectively.

From (37) to (39), it could be analyzed that (43) is the sufficient condition of (39)

$$\frac{V_o}{nV_{bus.avg}} = \frac{\left(D_{g.\min}^{KL\,\min} + 0.5\right)\sqrt{1 - \frac{K_{L\,\min}P_{o.\max}}{\eta\omega_l C_{bus}V_{bus.\mathrm{avg}}^{\ 2}}}}{1 + \frac{L_k}{L_m} + \frac{4n^2L_k f_s K_{L\,\min}P_{o.\max}}{V_o^2}} = \frac{0.673}{1 + \frac{L_k}{L_m} + \frac{4n^2L_k f_s K_{L\,\min}P_{o.\max}}{V_o^2}} \tag{43}$$

The normalized voltage transfer gain from $V_{bus.avg}$ to V_o is also expressed as

$$\frac{V_o}{nV_{bus.avg}} = \left[\begin{array}{l}\left(D_g + D_b\right) - \left(D_g - D_b\right)^2 \\ + \left|D_g - D_b\right|\left(1 - D_g - D_b\right)\end{array}\right]_{\substack{D_g = D_g^{KL\,\min} \\ D_b = D_b^{KL\,\min}}} \times \frac{\sqrt{1 - \frac{K_{L\,\min}P_{o.\max}\sin(2\omega_l t)}{\eta\omega_l C_{bus}V_{bus.\mathrm{avg}}^{\ 2}}}}{1 + \frac{L_k}{L_m} + \frac{4n^2L_k f_s K_{L\,\min}P_{o.\max}}{V_o^2}} \tag{44}$$

where $D_g^{KL\_min}$ and $D_b^{KL\_min}$ are D_g and D_b values in K_{L_min} load condition. Combining (43) and (44), the corresponding $D_b^{KL\_min}$ for a specific $D_g^{KL\_min}$ could be calculated. Hence, for minimum and maximum $D_g^{KL\_min}$ values, the corresponding $D_b^{KL\_min}$ values and instantaneous time t are calculated as

$$\begin{aligned} &D_g^{KL\,\min} = D_{g.min}^{KL\,\min} = 0.179 \\ &\Rightarrow D_b^{KL\,\min} = 0.487, t = \frac{1}{\omega_l}\tan^{-1}\left(\frac{\eta\omega_l C_{bus}V_{bus.\mathrm{avg}}^{\ 2}}{K_{L\,\min}P_{o.\max}}\right) \\ &D_g^{KL\,\min} = D_{g.\max}^{KL\,\min} = 0.334 \\ &\Rightarrow D_b^{KL\,\min} = 0.338, t = 0 \end{aligned} \tag{45}$$

From (27) and (45), the product of n and L_k is calculated to be larger than 24.0 μH. L_m is designed 10 times of L_k. From (43), n, L_k, and L_m are designed as 0.56, 50.0, and 500.0 μH, respectively.

3.4 | Output inductor and capacitor (L_o and C_o)

i_{Lo} is required to operate in CCM condition when the load condition is above or equal to the minimum allowable load condition K_{L_min}. Hence, from (13) and (45), the limitation of L_o is calculated to be larger than 178.4 uH. Finally, L_o is designed as 250 μH, and C_o is designed to be 60 μF to filter the ripple with switching frequency (50 kHz).

TABLE 1 Design summary of the laboratory prototype

Parameter	Values	Parameter	Values
$P_{o.\max}$	2 kW	L_o, C_o	250 μH, 60 μF
V_o	200 V	C_{bus}	240 μF, 800 V
v_s	198–242 V_{rms}, 50 Hz	L_{if}, C_{if}	330 μH, 1 μF
$V_{bus.avg}$	600 V	D_{R1}, D_{R2}	STTH6010
f_s	50 kHz	$Q1$–$Q4$	C2M0080120D
L_{in}	95.0 μH	D_{s1}, D_{s2}	C4D40120D
L_k, L_m	50 μH, 500 μH	Transducers	AMC1301DWVR
n (N_2/N_1)	0.56	Control unit	TI DSP F28335
C_d	1.5 μF, 500 V	Mosfet driver	CREE CRD-001

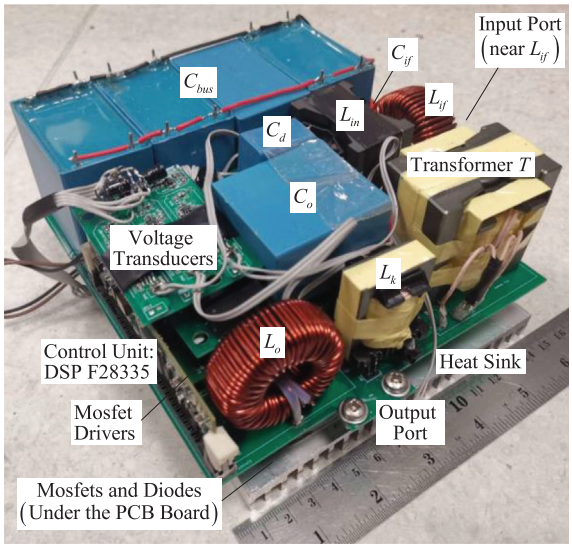

FIGURE 7 Laboratory prototype

3.5 | Soft-switching requirement: snubber capacitor C_s and switching deadtime T_{dt}

The critical current I_{crit} for ZVS would occur in K_{L_min} load condition. The calculation of I_{crit} is based on the condition of $D_a \geq D_b$. Hence, D_a and D_b used to calculate I_{crit} are expresses as

$$D_a = \begin{cases} \max\left(D_g^{KL\,\min}, D_b^{KL\,\min}\right) & D_g^{KL\,\min}, D_b^{KL\,\min} \leq 0.5 \\ \max\left(\left(1 - D_g^{KL\,\min}\right), \left(1 - D_b^{KL\,\min}\right)\right) & D_g^{KL\,\min}, D_b^{KL\,\min} > 0.5 \end{cases} \tag{46}$$

$$D_b = \begin{cases} \min\left(D_g^{KL\,\min}, D_b^{KL\,\min}\right) & D_g^{KL\,\min}, D_b^{KL\,\min} \leq 0.5 \\ \min\left(\left(1 - D_g^{KL\,\min}\right), \left(1 - D_b^{KL\,\min}\right)\right) & D_g^{KL\,\min}, D_b^{KL\,\min} > 0.5 \end{cases} \tag{47}$$

From (45) to (47), D_a and D_b are confirmed. Then, from (11), (14), (15), (17), (18), (27), and (33), I_{crit} is calculated as 4.34 A.

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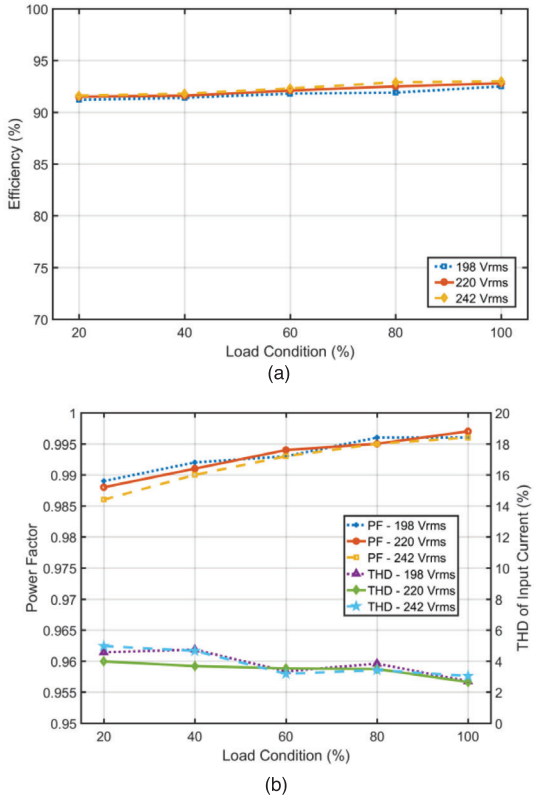

FIGURE 8 Performances in different load and line conditions: (a) efficiency; (b) power factor and THD of input current. THD, total harmonic distortion.

TABLE 2 Power loss breakdown of the proposed topology in 100% load condition

Component/device	Power loss breakdown
Input filter inductor	4.5%
Front-end diodes	13.1%
Input inductor	7.9%
Switches	21.2%
Primary inductor	6.1%
Transformer	19.4%
Secondary-side diodes	14.8%
Output inductor	13.0%
Efficiency	92.8%
Output power	2000 W

T_{dt} is set as 0.3 μs. From (28), C_s is limited to be smaller than 543 pF. Finally, C_s is designed as 470 pF.

3.6 | Design summary

Table 1 gives the design summary of the experimental prototype and Figure 7 shows the laboratory setup. The PI controller

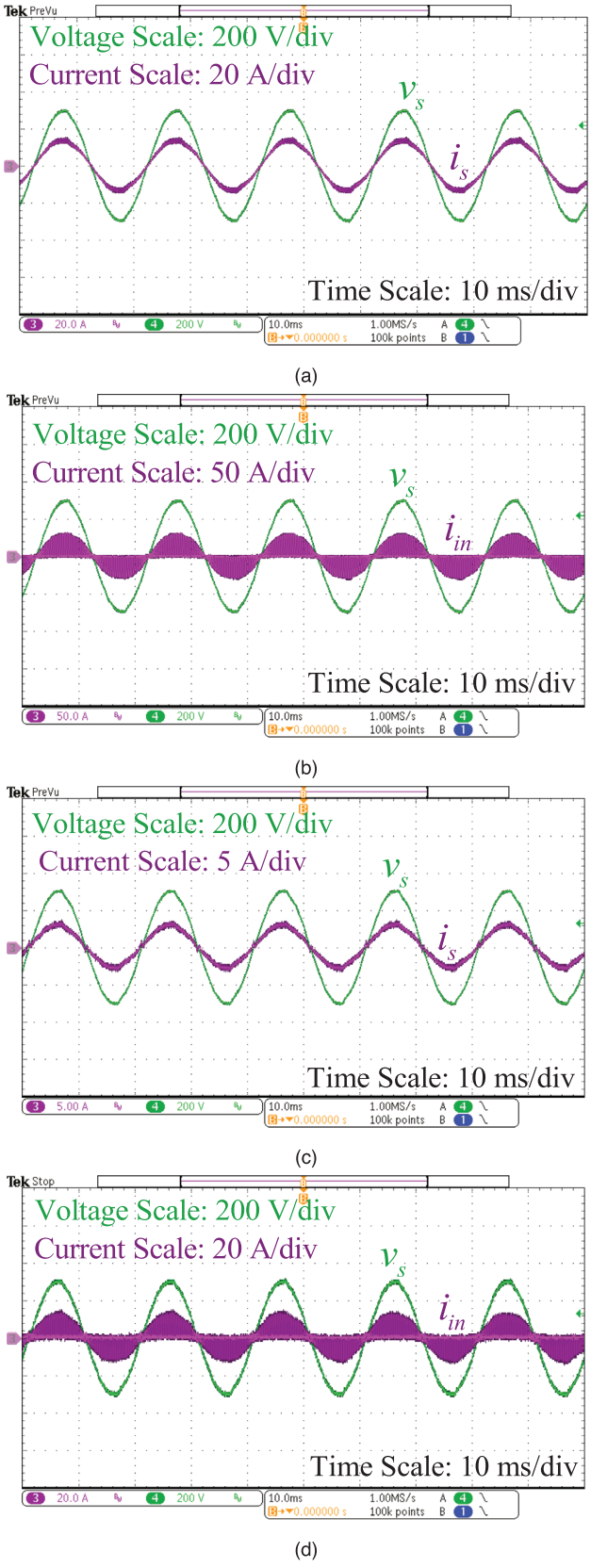

FIGURE 9 Waveforms at 220 V_{rms} line input: (a) input voltage v_s and input current i_s in 100% load condition; (b) input voltage v_s and input inductor current i_{in} in 100% load condition; (c) input voltage v_s and input current i_s at 20% load condition; (d) input voltage v_s and input inductor current i_{in} at 20% load condition

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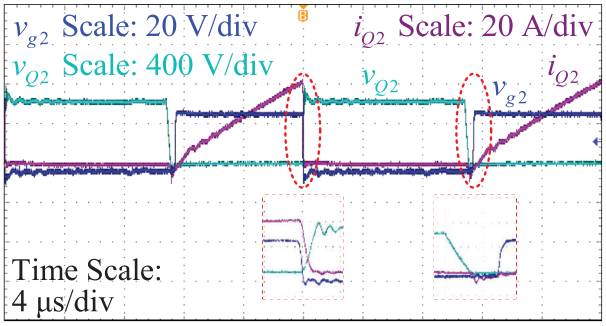

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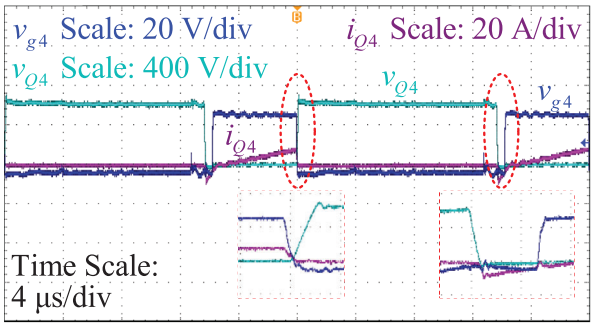

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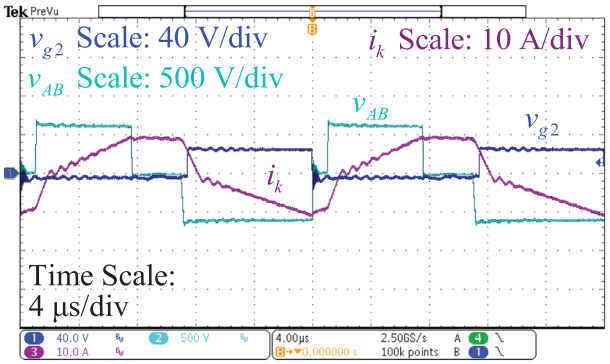

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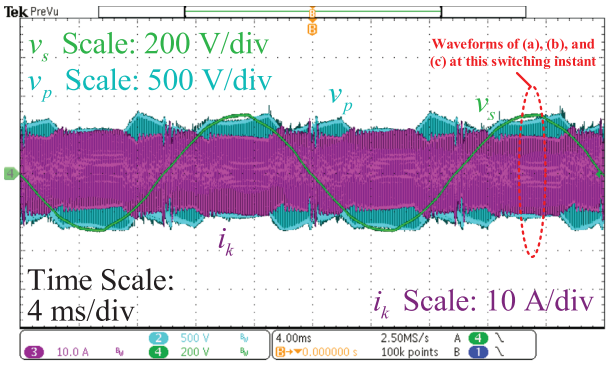
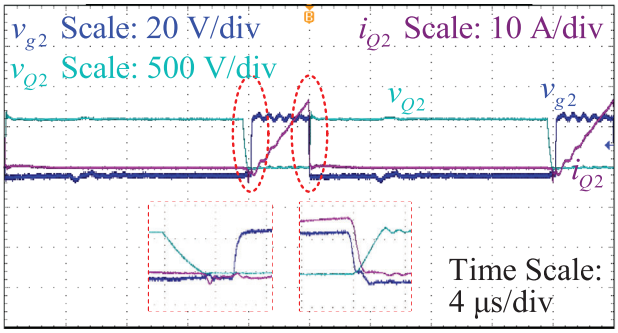


(d)

FIGURE 10 Waveforms at 220 V_{rms} line input and 100% load condition: (a) soft-switching waveforms of switch Q_2; (b) soft-switching waveforms of switch Q_4; (c) waveforms of v_{AB}, i_k, and v_{g2} at a switching instant; (d) overall waveforms of v_s, v_p, and i_k (low-frequency profile)



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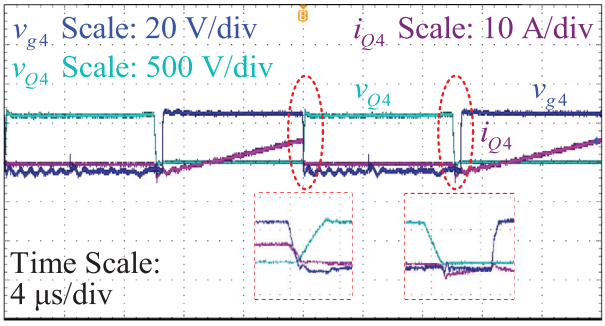

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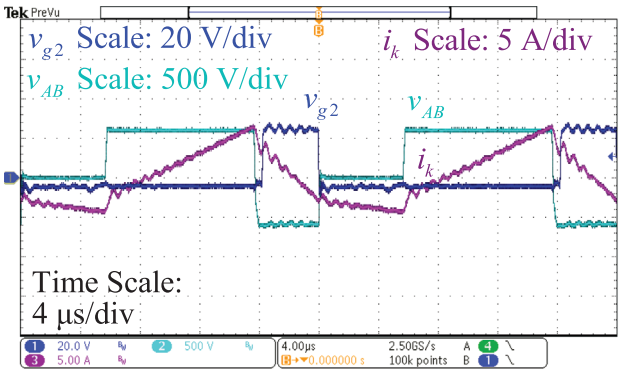

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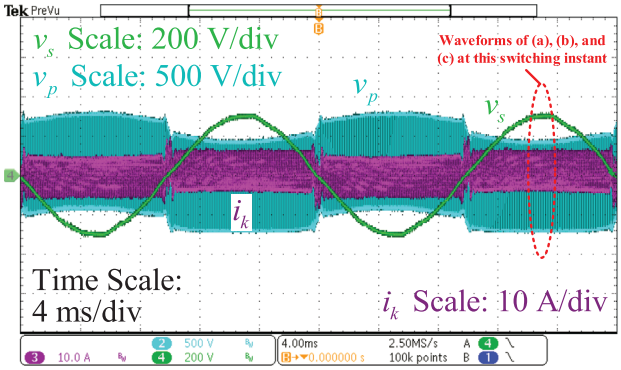

(d)

FIGURE 11 Waveforms at 220 V_{rms} line input and 20% load condition: (a) soft-switching waveforms of switch Q_2; (b) soft-switching waveforms of switch Q_4; (c) waveforms of v_{AB}, i_k, and v_{g2} at a switching instant; (d) overall waveforms of v_s, v_p, and i_k (low-frequency profile)

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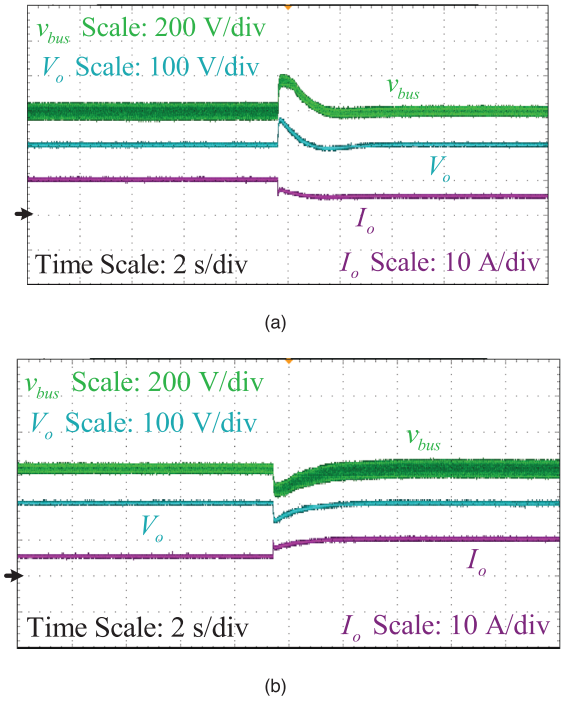

FIGURE 12 (a) Step response of v_{bus} and V_o from 100% to 50% load condition; (b) step response of v_{bus} and V_o from 50% to 100% load condition

parameters of the V_o control loop are designed to be 0.15 and 10, respectively. The PI controller parameters of the $V_{bus.avg}$ control loop are designed to be 0.0001 and 0.002, respectively.

4 | EXPERIMENTAL RESULTS

Experiments in 20% to 100% load conditions are tested to verify its functionalities and advantages. Figure 8 shows the measured overall efficiency, PF, and THD of input current (THD_i) in different load and input line conditions. In maximum load condition with 220 V_{rms} input voltage, the efficiency, PF, and THD_i can achieve the performances of 92.8%, 0.997, and 2.65%, respectively. From 20% to 100% load range, the overall efficiency maintains higher than 91%, the PF is over 0.986, and THD_i is below 5%. In general, the input power quality maintains a significantly high level within a wide load range. Figure 9 shows the waveforms of AC line input voltage, input current, and input inductor current in 100% and 20% load conditions with 220 V_{rms} line input. Table 2 presents the power loss breakdown in 100% load condition.

In 100% load condition, the high-frequency profiles of soft-switching waveforms of switches Q_2 and Q_4, as well as the operation waveforms of v_{AB} and i_k, are shown in Figures 10a to 10c, while Figure 10d shows the low-frequency profile of v_p and i_k. In 20% load condition, the high-frequency profiles of soft-switching waveforms of switches Q_2 and Q_4, as well as the waveforms of v_{AB} and i_k, are shown in Figures 11a to 11c, while Figure 11d shows the low-frequency profile of v_p and i_k. The switching waveforms of Q_1 and Q_3 are neglected because they are complementary with those of Q_2 and Q_4 respectively. Figure 12 shows the dynamic responses of the proposed converter.

TABLE 3 Comparisons with state-of-the-art single-phase single-stage isolated AC–DC topologies

Topologies/ methods	Efficiency (%) (load range)	Count of power devices	PF	THD_i (%)	Bus voltage	Power (W)	Constant or varying switching frequency	Capacitance (bus and output capacitors) per Watt
Proposed Method	91.2–93.0 (20%–100% load)	4 Mosfets + 4 diodes	0.997	2.65	Stable	2000	Constant	0.15 μF/W
Topology [19]	85.8–91.2 (31%–100% load)	2 Mosfets + 6 diodes	0.993	9.7	Stable	75	Constant	> 2.9 μF/W
Topology [20]	90.8–92.8 (70%–100% load)	2 Mosfets + 6 diodes	0.99	8.0	Unstable	100	Varying	3.3 μF/W
Topology [21]	80.0–96.2 (10%–100% load)	4 Mosfets + 6 diodes	0.998	3.91	Unstable	1000	Constant	1.52 μF/W
Topology [23]	87.0–92.5 (13%–100% load)	4 Mosfets + 6 diodes	0.981	5.6	Stable	1500	Constant	3.2 μF/W
Topology [33]	79.0–90.5 (20%–100% load)	4 Mosfets + 11 diodes	0.995	12.5	Unstable	1000	Constant	1.1 μF/W
Topology [35]	93.0–94.0 (50%–100% load)	5 Mosfets + 13 diodes	0.996	5.2	Not reported	3000	Constant	1.1 μF/W
[37]	87–90 (25%–100% load)	2 Mosfets + 6 diodes	0.997	6.0	Unstable	160	Varying	4.4 μF/W
[38]	92.7% (100% load)	4 Mosfets + 8 diodes	>0.98	Not reported	500/265	300	Varying	2.6 μF/W
[39]	94% (100% load)	6 Mosfets + 4 diodes	0.970	9.1	400/110	3300	Varying	0.28 μF/W

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Table 3 presents the comparisons of the proposed topology with other state-of-the-art single-stage AC–DC topologies in terms of efficiency, count of power semiconductor devices, power quality, power level, bus capacitor, output capacitor etc. As compared with other topologies, the proposed topology with the proposed modulation method utilizes the least power semiconductor devices and achieves better PFC performances. Most obviously, the total capacitance used for bus and output capacitors per Watt is much smaller than other existing single-stage topologies, which means that the polypropylene film capacitors can be used instead of bulky electrolytic capacitors. In general, the proposed modulation and method for the bridgeless single-stage full-bridge AC–DC converter exhibit significant and dominant advantages considering the integrated performances of different aspects as compared with other existing single-phase single-stage AC–DC topologies.

5 | CONCLUSION

A new asymmetric modulation method for bridgeless single-stage full-bridge AC–DC converter is proposed to improve input power quality and achieve soft-switching operation. Moreover, bulky bus and output capacitors can be eliminated. Besides, the advantages of reduced conduction loss and a small amount of power semiconductor devices are maintained. Descriptions and analysis of the topology, modulation method, operation principle, and control method are given in detail. Moreover, the specific design procedure is presented and a laboratory prototype with 2-kW output power is implemented. The experimental results demonstrate the functionalities and performances of the proposed converter and verify the correctness of the theoretical analysis and design.

AUTHOR CONTRIBUTIONS

Junwei Liu: Conceptualization; Formal analysis; Methodology; Validation; Writing—original draft. K. H. Loo: Funding acquisition; Supervision; Writing - review & editing. Guibin Wang: Supervision; Writing—review & editing. Xian Zhang: Funding acquisition; Supervision; Writing—review & editing. Ting Wu: Writing—review & editing.

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CONFLICT OF INTEREST

The authors do not have a conflict of interest.

DATA AVAILABILITY STATEMENT

Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

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